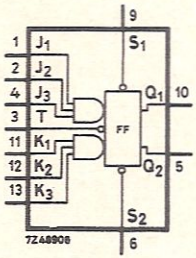
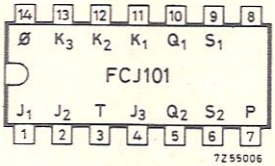
The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

# SINGLE JK FLIP-FLOP



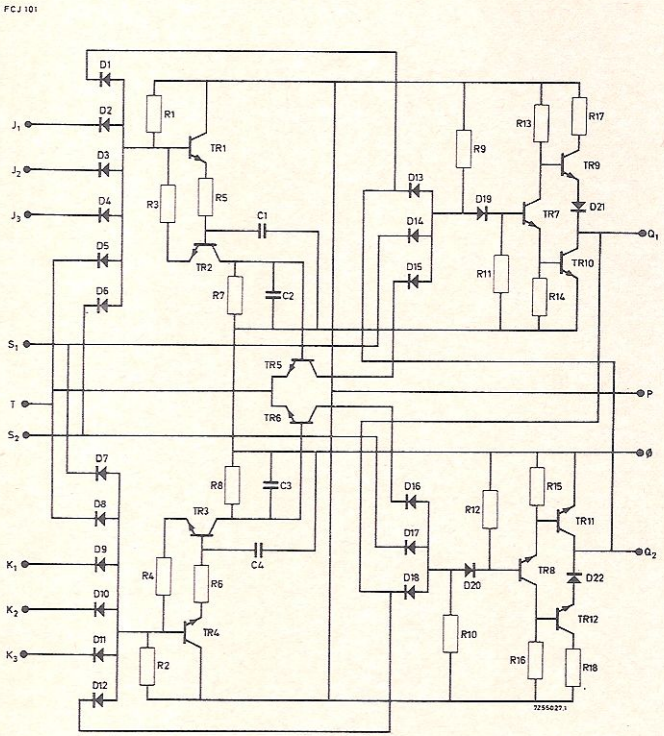

Package XG14; dual in-line

| QUICK REFERENCE DATA | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | 6.0 ± 5% | V |
| Operating ambient temperature range | $T_{amb}$ | 0 to +75 | °C |
| Clock rate | $f_c$ | typ. 10 | MHz |
| Available d.c. fan out<br>$T_{amb}$ = 0 to +75 °C | $N_a$ | ⩾ 8 | |
| D.C. noise margin<br>$T_{amb}$ = 25 °C | $M_L$ | typ. 1.2 | V |
| Power consumption<br>50% duty cycle, $T_{amb}$ = 25 °C | $P_{av}$ | typ. 36 | mW |

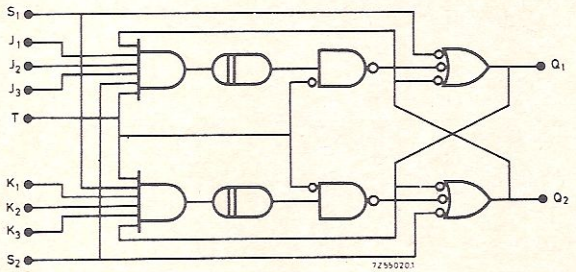
The FCJ101 performs the JK flip-flop operation. Three J and three K inputs permit an additional AND operation. Triggering occurs at the falling edge of a T signal. The direct-set inputs (overriding any other inputs) are active at the LOW level. The circuitry incorporates bi-directional outputs for driving capacitive loads. Typical applications are in high speed counters and shift registers.

Red binder Integrated circuits

## CIRCUIT DIAGRAM




## LOGIC DIAGRAM (to MIL standard 806B)



## FUNCTION TABLES

1. Trigger action via T terminal

| T = HIGH | | T = LOW | |
|---|---|---|---|
| J | K | $Q_1$ | $Q_2$ |
| H | H | reversed | |
| L | H | L | H |
| H | L | H | L |
| L | L | no change | |

The information on J and K is transferred into the flip-flop by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs $S_1$ and $S_2$ should be HIGH or floating.

$J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$
} for positive logic

2. Set or reset via S terminals

| $S_1$ | $S_2$ | $Q_1$ | $Q_2$ |
|---|---|---|---|
| H | L | L | H |
| L | H | H | L |
| L | L | H | H |
| H | H | no change | |

The set inputs override the other inputs and directly determine the outputs of the flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

## RATINGS (Limiting values) [1]

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | max. | 8.0 | V |
| Output voltage | $V_Q$ | max. | 8.0 | V |
| Input voltage | $V_J, V_K, V_T, V_S$ | max. | 8.0 | V |
| Output current [2] | $-I_Q$ | max. | 20 | mA |
| Input current [3] | $-I_J, -I_K, -I_T, -I_S$ | max. | 20 | mA |
| Voltage difference between any two inputs | | max. | 8.0 | V |
| Storage temperature | $T_{stg}$ | −55 to +125 | | °C |
| Operating ambient temperature | $T_{amb}$ | 0 to +75 | | °C |

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state.
3) At this limit input voltage typ. : −1.5 V.

## SYSTEM DESIGN DATA

| | | | | |
|---|---|---|---|---|
| Uniform system temperature | $T_{amb}$ | | 0 to +75 | °C |
| Uniform system supply voltage | $V_P$ | | 5.7 to 6.3 | V |
| Available d.c. fan out | | | | |
| to J or K input | $N_{aJ} = N_{aK}$ | ⩾ | 8 | |
| to S input | $N_{aS}$ | ⩾ | 4 | |
| to G input | $N_{aG}$ | ⩾ | 8 | |
| Available a.c. fan out | | | | |
| to T input | $N_{aT}$ | ⩾ | 2 | |
| D.C. noise margin | | | | |
| to T input | $M_L$ | min. | 0.3 | V |
| | $M_H$ | min. | 0.2 | V |
| to J or K input | $M_L$ | min. | 0.5 | V |
| | $M_H$ | min. | 0.2 | V |
| to S input | $M_L$ | min. | 0.3 | V |
| | $M_H$ | min. | 0.2 | V |
| to G input | $M_L$ | min. | 0.4 | V |
| | $M_H$ | min. | 1.5 | V |
| Average propagation delay time | $t_{pd}$ | max. | 85 | ns |
| Maximum clock rate | $f_c$ | ⩾ | 6 | MHz |
| Equivalent input capacitances | | | | |
| for T input | $C_T$ | typ. | 30 | pF |
| for J or K input | $C_J = C_K$ | typ. | 20 | pF |
| for S input | $C_S$ | typ. | 25 | pF |
| Supply current (duty cycle 50%) | $I_{Pav}$ | typ. | 6.0 | mA |
| Power dissipation at $T_{amb}$ = 75 °C | $P_{tot}$ | max. | 56 | mW |

## CHARACTERISTICS

| | | $T_{amb}$ (°C) | | | Conditions and references | |
|---|---|---|---|---|---|---|
| | | 0 | +25 | +75 | $V_P$ (V) | |
| STATIC DATA | | | | | | |
| Output voltage LOW | $V_{QLmax}$ | 0.4 | 0.4 | 0.4 V | 5.7 and 6.3 | |
| at: Output current LOW | $I_{QLmax}$ | 14.0<br>16.0 | 16.5<br>19.0 | 12.4 mA<br>14.4 mA | 5.7<br>6.3 | |
| Output voltage HIGH | $V_{QHmin}$ | 3.8 | 3.9 | 4.1 V | 5.7 | $I_Q = -100\ \mu A$ |
| Output voltage HIGH (lowest permissible) | $V_{QHPmin}$ | 3.6 | 3.3 | 3.0 V | 5.7 | |
| at: Output current HIGH | $-I_{QHmax}$ | 0.85 | 3.3 | 5.5 mA | 5.7 | |
| Input current LOW | $-I_{JLmax}$, $-I_{KLmax}$ | 1.75<br>2.0 | 1.65<br>1.9 | 1.55 mA<br>1.8 mA | 5.7<br>6.3 | $V_J = V_K = 0.4$ V<br>$V_J = V_K = 0.4$ V |
| | $-I_{TLmax}$ | 3.5<br>4.0 | 3.3<br>3.8 | 3.1 mA<br>3.6 mA | 5.7<br>6.3 | $V_T = 0.4$ V<br>$V_T = 0.4$ V |
| | $-I_{SLmax}$ | 3.5<br>4.0 | 3.3<br>3.8 | 3.1 mA<br>3.6 mA | 5.7<br>6.3 | $V_S = 0.4$ V<br>$V_S = 0.4$ V |
| Input current HIGH | $-I_{JHmax}$, $-I_{KHmax}$ | 1 | 1 | 25 $\mu$A | 5.7 | $V_J = V_K = 5.3$ V other inputs 0 V |
| | $I_{THmax}$ | 2 | 2 | 50 $\mu$A | 5.7 | $V_J = 5.3$ V other inputs 0 V |
| | $I_{SHmax}$ | 2 | 2 | 50 $\mu$A | 5.7 | $V_S = 5.3$ V other inputs 0 V |
| Supply current | $I_{Pmax}$ | – | 9 | – mA | 6.3 | T input LOW J, K, S inputs HIGH |

## CHARACTERISTICS

| | | $T_{amb}$ (°C) | | | | Conditions and references | | |
|---|---|---|---|---|---|---|---|---|
| | | 0 | +25 | +75 | | $V_P$ (V) | | fig. |
| DYNAMIC DATA | | | | | | 5.7 and 6.3 | | |
| Change of state | | | | | | | | |
| Input voltage HIGH during: | $V_{THmin}$ $V_{JHmin}$ $V_{KHmin}$ | 3.6 | 3.3 | 3.0 | V | | HIGH level at T and J and/or K to be present simultaneously | 1 |
| Input time HIGH | $t_{THmin}$ | 50 | 50 | 50 | ns | | | 1 |
| followed by: T-input slope | $(-\frac{dt}{dV})_{Tmax}$ | 18 | 18 | 18 | ns/V | | | 1 |
| | $(-\frac{dt}{dV})_{Tmin}$ | 4 | 4 | 4 | ns/V | | | 1 |
| to: T-input voltage LOW | $V_{TLmax}$ | 0.7 | 0.7 | 0.7 | V | | $t_{TLmin} = t_{pdf}$ | 1 |
| No change of state | | | | | | | | |
| JK-input voltage LOW during: | $V_{JLmax}$ $V_{KLmax}$ | 1.1 | 1.0 | 0 9 | V | | J and K turning LOW after T and J and/or K having | 2 |
| JK-input time LOW | $t_{JLmin}$ $t_{KLmin}$ | 100 | 100 | 160 | ns | | been HIGH simultaneously | 2 |
| Clock skew protection | | | | | | | | |
| Hold time LOW | $t_{holdLmax}$ | 15 | 15 | 15 | ns | | | 2 |
| Hold time HIGH | $t_{holdHmax}$ | 7 | 10 | 10 | ns | | | 3 |
| Set or Reset | | | | | | | | |
| S-input voltage LOW | $V_{SLmax}$ | 1.0 | 0.9 | 0.7 | V | | active $t_{SLmin} = t_{pdf}$ | 4 |
| S-input voltage HIGH | $V_{SHmin}$ | 3.6 | 3.3 | 3.0 | V | | inactive | |
| Propagation delay times from T to Q | | | | | | | | |
| Rise propagation delay time | $t_{pdr\,max}$ | – | 70 | – | ns | 6.0 | $V_{pd}$ = 1.5 V N = 1; $C_L$ = 60 pF | 5 |
| Fall propagation delay time | $t_{pdf\,max}$ | – | 100 | – | ns | 6.0 | $V_{pd}$ = 1.5 V N = 8; $C_L$ = 60 pF other output N = 1 $C_L$ = 60 pF | 5 |

## CHARACTERISTICS (continued)

### DYNAMIC DATA

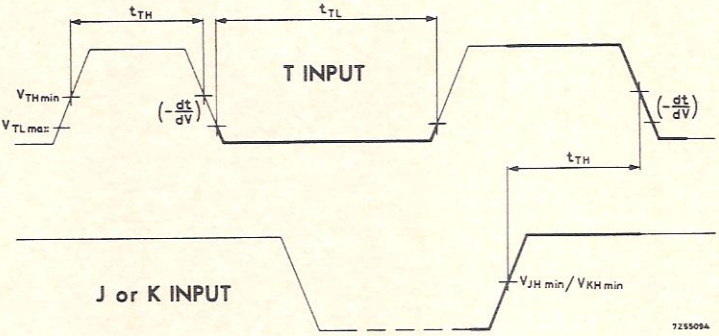



Fig.1. Waveforms illustrating conditions for change of state.

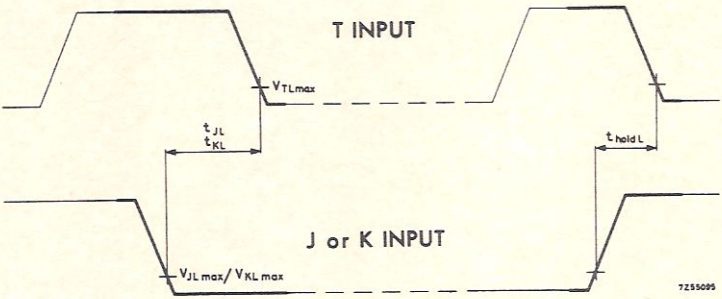



Fig.2. Waveforms illustrating conditions for no change of state.

For no change of state to result:

a. the time between J or K reaching $V_{JLmax}$, $V_{KLmax}$ (going LOW) and T reaching $V_{TLmax}$ (going LOW) must be at least $t_{JLmin}$, $t_{KLmin}$.

b. the time between J or K reaching $V_{JLmax}$, $V_{KLmax}$ (going HIGH) and T reaching $V_{TLmax}$ (going LOW) must be less than $t_{holdL}$.

CHARACTERISTICS (continued)

DYNAMIC DATA

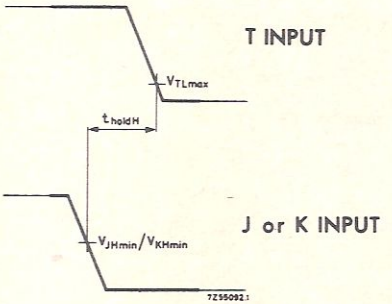



Fig.3. Waveforms illustrating conditions for change of state.
For a change of state still to result, the time between J or K reaching $V_{JHmin}$, $V_{KHmin}$ (going LOW) and T reaching $V_{TLmax}$ (going LOW) must be less than $t_{holdH}$

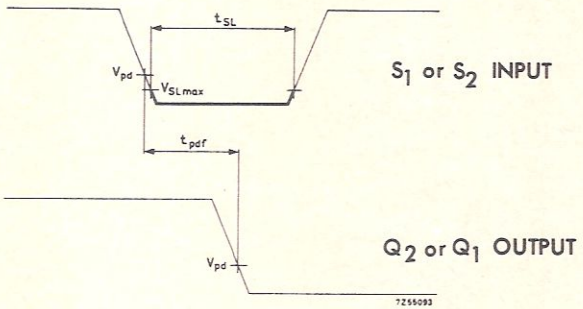
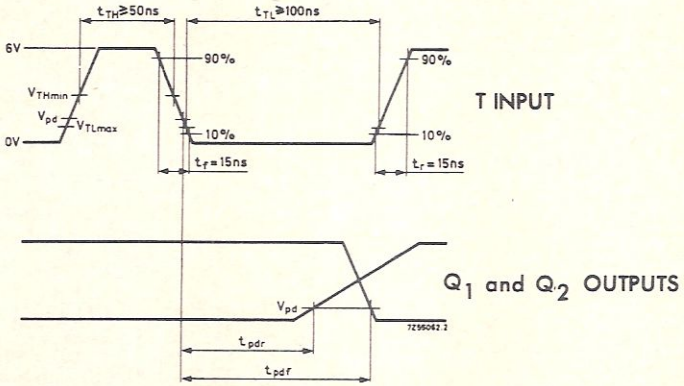
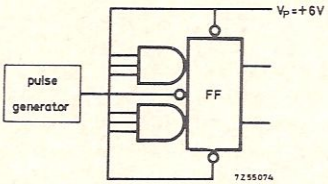



Fig.4. Waveforms illustrating conditions for set or reset.

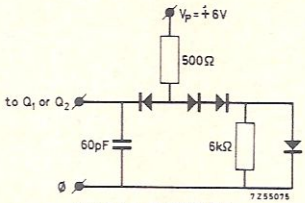
**CHARACTERISTICS** (continued)

DYNAMIC DATA



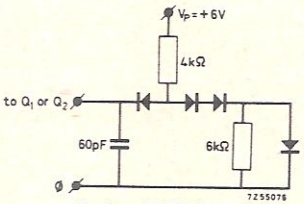




$C_L = C_W + C_i (N - 1)$




diodes FCY101

Equivalent load for N = 8 and $C_W$ = 30 pF



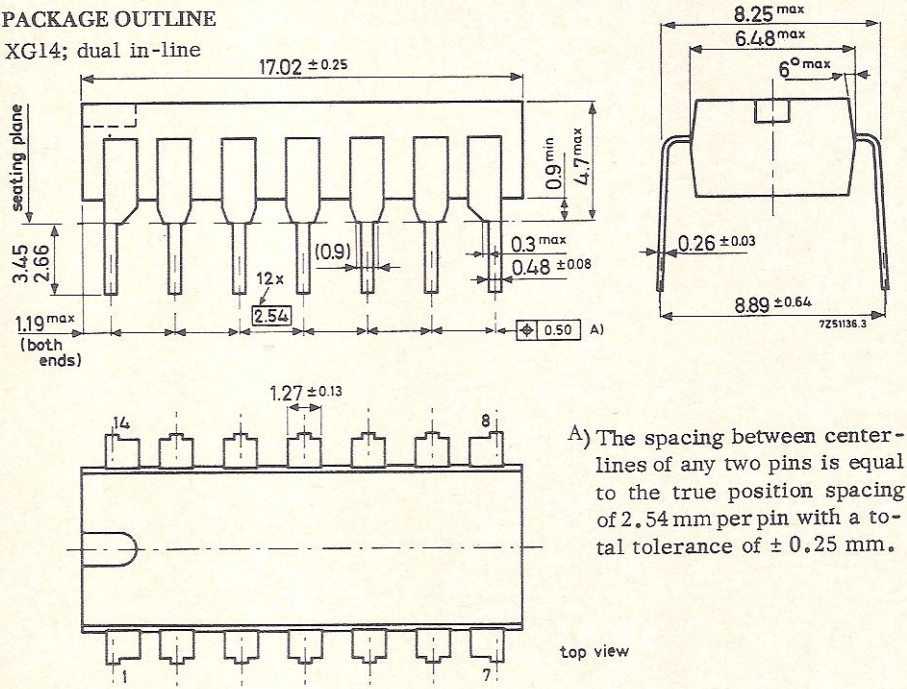

diodes FCY101

Equivalent load for N = 1 and $C_W$ = 60 pF

Fig. 5. Waveforms and loading circuits illustrating measurement of $t_{pdr}$ and $t_{pdf}$.

## PACKAGE OUTLINE

XG14; dual in-line




A) The spacing between centerlines of any two pins is equal to the true position spacing of 2.54 mm per pin with a total tolerance of ± 0.25 mm.

## HANDLING NOTES

1. Devices may be soldered directly into circuits with soldering irons. At iron temperatures below 245 °C the maximum soldering time should be less than 10 seconds and at iron temperatures between 245 °C and 400 °C the soldering time should be less than 5 seconds. In both cases the soldering iron should be applied below the seating plane.

2. Devices mounted up to the seating plane on a printed circuit board may be dip or flow soldered providing the solder temperature is below 245 °C and the time of immersion is less than 5 seconds. The body temperature should not be allowed to exceed the maximum storage temperature during soldering. If excessive preheat cycles are used, it may be necessary to cool the printed board immediately after leaving the solder bath/wave in order that this requirement be met.